REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1, 3-6, 10, 13, 14 and 16-28 are in this case. Claims 1, 3, 4, 6, 10, 13, 14 and 16-28 have been rejected under § 102(e). Claim 5 has been rejected under § 103(a). Independent claims 13, 14, 16 and 17 and dependent claims 22 and 23 have been amended. New dependent claims 29 and 30 have been added.

The claims before the Examiner are directed toward a non-volatile memory device for storing both code and data. While the device is programming or erasing its nonvolatile memory, if a host system sends the device a read request, hardware such as one or more logic circuits in the device signals the host to delay executing the request while the device suspends the programming/erasing. Then the hardware suspends the programming/erasing and signals the host to execute the read request. When all read requests have concluded, the hardware resumes the programming/erasing.

§ 102(e) Rejections – See et al. '070

The Examiner has rejected claims 1, 3, 4, 6, 10, 13, 14 and 16-28 under § 102(e) as being anticipated by See et al., US Patent No. 6,189,070 (henceforth, "See et al. '070"). The Examiner's rejection is respectfully traversed.

Like the present invention, See et al. '070 teach a memory device **410** whose programming/erasing operations are suspended when processor **402** that accesses device **410** needs to read data from device **410**. (Note that the processor in Figure 2 is labeled "**400**". This is an error. The reference numeral that is used consistently in the text of See et al. '070 for the processor is "**402**".) The difference between the present invention and the invention of See et al. '070 lies in which component is responsible

for initiating the suspensions of programming/erasing operations. In See et al. '070 processor **402** is responsible for signaling device **410** explicitly to initiate suspension and resumption of the programming/erasing operations as needed. This is in contrast to the present invention, in which hardware in the memory device itself initiates the suspension and resumption of the programming/erasing operations in response to read requests from the host system.

It is clear from See et al. '070 that it is their processor **402**, and not the hardware in signaling device **410** such as circuitry **190**, **192**, **194** and **195**, that takes the initiative in suspending and resuming programming/erasing operations. This aspect of the invention of See et al. '070 is clearest in their claims, for example claim 6:

> A system comprising:
> a processor;
> a nonvolatile writeable memory having an array, the nonvolatile writeable memory having a first mode for allowing the array to be written to, and a second mode for allowing the array to be read from, the nonvolatile writeable memory storing low level code which <u>when executed by the processor cause the processor to perform</u>:
> (a) disabling interrupts;
> (b) initiating a non-read operation to the nonvolatile writeable memory while the array is in the first mode and, wherein, the non-read operation is initiated by low-level routines downloaded to a volatile memory from the nonvolatile writeable memory;
> (c) checking for interrupts, and in response to detecting an interrupt performing:
> (i) <u>suspending the non-read operation</u>;
> (ii) placing the array in the second mode;
> (iii) enabling interrupts; and
> (iv) reading code from the nonvolatile writeable memory. (emphasis added)

and 11:

A computer-readable medium having stored thereon a plurality of instructions which, when executed by a processor, cause the processor to perform:

(a) disabling interrupts

(b) initiating a non-read operation to the nonvolatile writeable memory while the array is in a first mode and, wherein, the non-read operation is initiated by low-level routines downloaded to a volatile memory from the nonvolatile writeable memory;

(c) checking for interrupts, and in response to detecting an interrupt performing the steps of:

(i) suspending the non-read operation;

(ii) placing the array in a second mode;

(iii) enabling interrupts; and

(iv) reading code from the nonvolatile writeable memory. (emphasis added)

This aspect of the invention of See et al. '070 also is clear from column 8 lines 65-67:

> The program suspend operation is initiated by writing a program suspend command to the command decoder **170**.

and from column 9 lines 5-7:

> The erase suspend operation may be initiated by writing an erase suspend command to the command decoder **170**.

Note in particular that from among the commands decoded by command decoder **170**, as listed in column 7 lines 50-52:

> ...(1) erase, (2) erase suspend, (3) erase resume, (4) program, (5) program suspend, (6) program resume, (7) read, and (8) read status

the "read" command is specifically not used to initiate the suspending and resuming of programming/erasing operations.

This distinction between the present invention and the teachings of See et al. '070 is recited quite clearly in independent claims 1 and 24. The last element recited in claim 1 is:

> logic circuit, separate from said host, for enabling automatic suspending and/or automatic resuming of operations in response to a read request from said host. (emphasis added)

The last two steps recited in claim 24 are:

during said operation, requesting a read operation, by the host; and
in response to said request, suspending said operation, by the memory device (emphasis added)

Independent claims 13, 14, 16 and 17 have been amended to more clearly recite this difference.

The first step of independent claim 13 has been amended to state that the logic circuit(s) is/are added to the non-volatile memory device, and is not merely added to "operate with" the non-volatile memory device. Support for this amendment is found in the specification in Figure 4 that shows automatic suspend logic **26** and automatic resume logic **27** inside the rectangle that bounds the non-volatile memory device. The first step of independent claim 13 as now amended, together with the last step of independent claim 13,

commanding the device to suspend and/or resume device operations in response to a read request, by said at least one logic circuit (emphasis added)

clearly distinguish the present invention from the teachings of See et al. '070.

The first step of independent claim 14 has been amended similarly. The first step of independent claim 14 as now amended, together with the second and third steps of independent claim 14,

sensing a read request while the device is in program/erase mode/operation, by said at least one logic circuit
in response to said sensing, entering of program and/or erase operations into suspended mode, by said at least one logic circuit (emphasis added)

clearly distinguish the present invention from the teachings of See et al. '070.

Claim 16 has been amended to state that the suspending of data processing operations is in response to at least one read request received by the memory device from a host. Support for this amendment is found in the specification on page 9 lines 1-2:

> Upon detection of the read operation **11** the automatic suspend logic **26** executes a process that enters the device into the suspend state **12**.

Note that read operation **11** is called a "read request" on page 6 line 19 of the specification. Page 6 line 22 of the specification identifies the "CPU/Bus" as the source of the read requests. On page 7 lines 10 and 11 of the specification, the "CPU/Bus" is called a "host". This amendment of independent claim 16 clearly distinguishes the present invention from the teachings of See et al. '070.

Independent claim 17 has been amended similarly, to state that the hardware mechanism is for suspending an activity of the circuitry in response to at least one read request received by the memory device from a host. This amendment of independent claim 17 clearly distinguishes the present invention from the teachings of See et al. '070. For consistency, "a host" has been amended to "said host" in dependent claim 22.

Thus, the present invention, as recited in independent claims 1, 13, 14, 16, 17 and 24, is not anticipated by See et al. '070. Furthermore, the present invention, as recited in independent claims 1, 13, 14, 16, 17 and 24, is not obvious from See et al. '070. There is neither a hint nr a suggestion in See et al. '070 that memory device **410** could or should be modified to relieve processor **402** of the burden of managing the suspension and resumption of programming/erasing operations.

With independent claims 1, 17 and 24 allowable in their present form, it follows that claims 3, 4, 6, 10, 18-23 and 25-28, that depend therefrom, also are allowable.

§ 103(a) Rejections – See et al. '070 and Keeley et al. '790

The Examiner has rejected claims 5 under § 103(a) as being unpatentable over See et al. '070 and Keeley et al., US Patent No. 4,491,790. The Examiner's rejection is respectfully traversed.

It is demonstrated above that independent claim 1 is allowable in its present form. It follows that claim 5, that depends therefrom, also is allowable.

Other Amendments to the Claims

Claim 23 has been amended to remove scaffolding that was inadvertently left behind after claim 23 was drafted.

New Claims

To emphasize the difference between the present invention and the teachings of See et al. '070, new dependent claims 29 and 30 have been added. New claim 29 states that the suspending of the erasing or programming operation, as recited in claim 24, is done only by the memory device. New claim 30 states that the resuming of the erasing or programming operation, as recited in claim 28, is done only by the memory device.

Support for these new claims is found in the specification in Figure 4 and the accompanying text. Figure 4 shows automatic suspend logic **26** and automatic resume logic **27** as components of the memory device, within the rectangle that encloses the other components (Bus I/F logic **23**, Flash array **24** and Flash circuitry **25**) of the memory device. Page 8 line 14 through page 9 line 14 describes how the entry to the suspend state is managed exclusively by automatic suspend logic **26**. Page 9 line 15 through page 10 line 5 of the specification describes how the

resumption of the suspended operation is managed exclusively by automatic resume logic **27**.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 13, 14, 16, 17 and 24, and hence dependent claims 3-6, 10, 18-23 and 25-30 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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